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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
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09/800,412 03/06/01 CHENG

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EXAMINER

MMC2/0817

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P.O. BOX 2903
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ALCALA, T
ART UNIT

PAPER NUMBER

2841
DATE MAILED:

08/17/01 *#3*

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary

Application No.

09/800,412

Applicant(s)

CHENG, YU-CHIANG

Examiner

Jose H Alcala

Art Unit

2841

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 06 March 2001.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-13 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-13 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413) Paper No(s). _____
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ 6) ☐ Other: _____

Art Unit: 2841

DETAILED ACTION***Double Patenting***

1. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

1-13

2. Claims ~~4-10~~ are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-10 of copending Application No. 09/799,900. Although the conflicting claims are not identical, they are not patentably distinct from each other because:

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Regarding Claim 1, copending Application No. 09/~~799,900~~ teaches a multi-layer circuit board comprising: first, second, third, fourth and fifth insulating substrates disposed sequentially one above the other; a first signal wiring layer disposed on one side of said first insulating substrate opposite to said second insulating substrate; a first ground wiring layer disposed between said first and second insulating substrates; a second signal wiring layer disposed between said second and third insulating substrates; a third signal wiring layer disposed between said third and fourth insulating

Art Unit: 2841

substrates; a power wiring layer disposed between said fourth and fifth insulating substrates; and a fourth signal wiring layer disposed on one side of said fifth insulating substrate opposite to said fourth insulating substrate; wherein said first, second, third, fourth and fifth insulating substrates, said first, second, third and fourth signal wiring layers, said ground wiring layer and said power wiring layer are press-bonded to each other to form said circuit board; wherein said first signal wiring layer has a first resistance with respect to said ground wiring layer, said second signal wiring layer having a second resistance with respect to said ground wiring layer and said power wiring layer, said third signal wiring layer having a third resistance with respect to said ground wiring layer and said power wiring layer, said fourth signal wiring layer having a fourth resistance with respect to said power wiring layer; and wherein said first, second, third and fourth resistances are within the range of 49.5 to 60.5 ohms.

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Application No. 09/~~799,900~~ fails to teach a sixth and seventh insulating substrates disposed sequentially above the other with the rest of the insulating substrates. In addition, it fails to teach that the fourth signal layer is located between the fifth and sixth insulating substrates. Additionally, it fails to teach a second ground wiring layer disposed between said sixth and seventh insulating substrates; and a fifth signal wiring layer disposed on one side of said seventh insulating substrate opposite to said sixth insulating substrate; wherein each of said first and seventh insulating substrates has a thickness ranging from 2.5 to 6.5 mil; wherein each of said second, fourth and sixth insulating substrates has a thickness ranging from 3 to 9 mil; wherein each of said third and fifth insulating substrates has a thickness ranging from 3 to 23 mil, a fifth

Art Unit: 2841

signal wiring layer having a fifth resistance with respect to said second ground wiring layer, and that the fifth resistance is within the range of 49.5 to 60.5 ohms.

It would have been obvious to one of ordinary skill in the art at the time of the invention to add a second ground layer and a fifth signal wiring layer with a fifth resistance with respect to said second ground wiring layer, in order to increase the current carrying capacity of the circuit board. It would have been further obvious and inherent to the circuit board to add a sixth insulating layers at the other side of the fourth signal wiring layer and a seventh insulating substrate at the other side of the second ground layer, in order to insulate the wiring layer eliminating any undesired current from flowing from one conducting layer to the other.

It would have been obvious to one of ordinary skill in the art at the time of the invention to make each of said first and seventh insulating substrates with a thickness ranging from 2.5 to 6.5 mil; and each of said second, fourth and sixth insulating substrates having a thickness ranging from 3 to 9 mil; and each of said third and fifth insulating substrates having a thickness ranging from 3 to 23 mil, a fifth signal wiring layer having a fifth resistance with respect to said second ground wiring layer, and that the fifth resistance is within the range of 49.5 to 60.5 ohms, in order to have more room for error and to change the thickness of the layers to make more rigid or less rigid by increasing or decreasing the value. Furthermore, it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art. See, *In re Aller*, 105 USPQ 233.

Art Unit: 2841

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Regarding claim 2, Application No. 09/~~799,900~~ claims at least one of said first; third and fifth insulating substrates is made from a polyester prepreg, but fails to claim the seventh insulating substrate as being made from that material. It would have been obvious to one of ordinary skill in the art at the time of the invention to make the seventh insulating substrate from the same material as the other substrates, to reduce the production costs and time, by eliminating the extra time and expense involved in getting a different material.

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Regarding claim 3, Application No. 09/~~799,900~~ claims at least one of said second and fourth insulating substrates is made from a fibrous core material, but fails to claim the sixth insulating substrate as being made from that material. It would have been obvious to one of ordinary skill in the art at the time of the invention to make the sixth insulating substrate from the same material as the other substrates, to reduce the production costs and time, by eliminating the extra time and expense involved in getting a different material.

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Regarding claims 4 and 5, Application No. 09/~~799,900~~ claims that the core material contains paper fibers, and that.

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Regarding claim 5, Application No. 09/~~799,900~~ claims that the core material contains glass fibers.

Art Unit: 2841

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Regarding claims 6, 7 and 8, Application No. 09/799,900 fails to teach that the thickness of each of said first and seventh insulating substrates are equal, that the thickness of said second and sixth insulating substrates are equal, and that the thickness of said third and fifth insulating substrates are equal. It would have been obvious to one having ordinary skill in the art at the time of the invention was made to make the thickness of each of said first and seventh insulating substrates equal, and to make the thickness of each of said second and sixth insulating substrates equal, and to make the thickness of each of said third and fifth insulating substrates equal, in order to make sure that the thermal expansion coefficient of every combination of two substrates are very similar, and in that way improving the adhesion and rigidity of the circuit board. In addition, it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. See, In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

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Regarding claim 9, Application No. 09/799,900 fails to teach that each of said first and fifth signal wiring layers has a thickness of about 1.4 mil; and each of said second, third and fourth signal wiring layers, said first and second ground wiring layers, and said power wiring layer has a thickness of about 0.7 mil. It would have been obvious to one having ordinary skill in the art at the time of the invention was made to make those changes in the thickness of the signal wiring layers, ground layers, and power layers in order to control the current conducting properties of the printed circuit board to a certain range of values. In addition, it has been held that discovering an

Art Unit: 2841

optimum value of a result effective variable involves only routine skill in the art. See, In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

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Regarding claim 10, Application No. 09/~~799,900~~ fails to teach that each of said third and fifth insulating substrates has a thickness ranging from 3 to 9 mil. It would have been obvious to one having ordinary skill in the art at the time of the invention was made to make each of said third and fifth insulating substrates having a thickness ranging from 3 to 9 mil, in order to have more room for error and to change the thickness of the layers to make more rigid or less rigid by increasing or decreasing the value. Furthermore, it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art. See, In re Aller, 105 USPQ 233.

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Regarding claim 11, Application No. 09/~~799,900~~ fails to teach that each of said first and seventh insulating substrates has a thickness of 4.5 mil; each of said second, third, fourth, fifth and sixth insulating substrates has a thickness of 6 mil; and that all the layers are press-bonded to each other to form said circuit board with a thickness of about 1.2 mm.

Art Unit: 2841

It would have been obvious to one having ordinary skill in the art at the time of the invention was made to make each of said first and seventh insulating substrates having a thickness of 4.5 mil; each of said second, third, fourth, fifth and sixth insulating substrates has a thickness of 6 mil, in order to make sure that the thermal expansion coefficient of the substrates in the middle are very similar and the ones at both ends are very similar, and in that way improving the adhesion and rigidity of the circuit board. In addition, it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. See, *In re Boesch*, 617 F.2d 272, 205 USPQ 215 (CCPA 1980). It would have been further obvious to form said circuit board with a thickness of about 1.2 mm, making the circuit board smaller in order to make it more lightweight and to decrease rigidity. In addition, it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. See, *In re Boesch*, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

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Regarding claim 12, Application No. 09/~~799,900~~ fails to teach that each of said third and fifth insulating substrates has a thickness ranging from 9 to 23 mil. It would have been obvious to one having ordinary skill in the art at the time of the invention was made to make each of said third and fifth insulating substrates having a thickness ranging from 9 to 23 mil, in order to have more room for error and to change the thickness of the layers to make more rigid or less rigid by increasing or decreasing the value. Furthermore, it has been held that where the general conditions of a claim are

Art Unit: 2841

disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art. See, In re Aller, 105 USPQ 233

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Regarding claim 13, Application No. 09/~~799,900~~ teaches that all the layers are press-bonded to each other to form said circuit board with a thickness of about 1.6 mm., but fails to teach that each of said first and seventh insulating substrates has a thickness of 4.5 mil; each of said second, third, fourth, fifth and sixth insulating substrates has a thickness of 6 mil.

It would have been obvious to one having ordinary skill in the art at the time of the invention was made to make each of said first and seventh insulating substrates having a thickness of 4.5 mil; each of said second, third, fourth, fifth and sixth insulating substrates has a thickness of 6 mil, in order to make sure that the thermal expansion coefficient of the substrates in the middle are very similar and the ones at both ends are very simmlar, and in that way improving the adhesion and rigidity of the circuit board. In addition, it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. See, In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

3. This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Art Unit: 2841

Conclusion

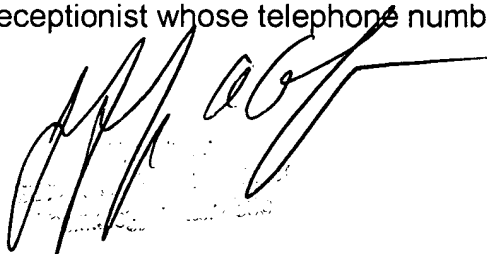
4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following references include elements from the instant claimed invention such as as alternating power and ground layers of different voltages and thickness: Iwane (US Patent No. 5,719,750), Kuwabara et al. (US Patent No. 4,675,789), and Skinner et al. (US Patent No. 6,191,475 B1).

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jose H Alcala whose telephone number is (703) 305-9844. The examiner can normally be reached from Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jeffrey Gaffin can be reached on (703) 308-3301. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 305-3431 for regular communications and (703) 305-3431 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

JHA
August 12, 2001

A handwritten signature in black ink, appearing to read "JH Alcala", is written over the typed name "Jose H Alcala" in the signature block.